AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 12 as follows:

In recent years, data processing apparatuses such as a CPU (Central-Processing Unit) and the like have become more widespread, and the demand to improve the processing speed of the data processing apparatus seems insatiable. In the conventional data processing apparatus such as a CPU, the instruction fetch mechanism, instruction decoding mechanism, instruction execution mechanism, and the like are set in a pipelined manner. The processing performance of the data processing apparatus is improved by increasing the frequency of the operating clock as well as reducing the access cycle of the memory to obtain memory access within one pipeline ~~stage~~ cycle time (one clock of the operating dock).

Please amend the paragraph beginning at page 2, line 21 as follows:

According to an aspect of the present invention, a data processing apparatus includes an instruction memory storing an instruction, a data memory storing data, an instruction decoder decoding a fetched instruction, a memory operation unit connected to the instruction memory, the data memory and the instruction decoder to fetch an instruction stored in the instruction memory to access the data memory according to the decoded result of the instruction decoder, and an integer operation unit carrying out an integer operation according to the decoded result of the instruction decoder. The instruction memory includes a plurality of instruction memory banks. The memory operation unit generates a pipeline ~~stage~~ cycle corresponding to selection of an instruction memory bank and a pipeline ~~stage~~ cycle corresponding to an instruction readout when an instruction is to be fetched from a plurality of instruction memory banks to carry out a pipeline process.

Please amend the paragraph beginning at page 3, line 2 as follows:

Since the memory operation unit generates a pipeline ~~stage~~ cycle corresponding to selection of an instruction memory bank and a pipeline ~~stage~~ cycle corresponding to an instruction readout, the selected instruction memory bank alone can be precharged. Therefore, power consumption can be reduced. Also, since the pipeline ~~stage~~ cycle corresponding to

selection of an instruction memory bank and the pipeline ~~stage~~ cycle corresponding to an instruction readout are effected in parallel, the throughput of the instruction memory access can be improved.

Please amend the paragraph beginning at page 15, line 20 as follows:

As shown in Figs. 14C and 14G, data transfer contention occurs at the data bus when the data memory is accessed at a plurality of pipeline ~~stages~~ cycles of M0-M2 or M0-Ml in the execution of the LD/ST instruction. Therefore, there was a problem that the store instruction cannot be executed immediately after execution of a load instruction. In the present embodiment, core 100 transfers data via data input bus 108 when the load instruction is executed and via data output bus 107 when the store instruction is executed. Therefore, the pipeline will not be disturbed even in the case where a store instruction is to be executed immediately after execution of a load instruction. Since the data transfer direction is predetermined in respective data buses, there is the advantage that the circuitry is simplified.

Please amend the paragraph beginning at page 21, line 14 as follows:

According to the data processing apparatus of the present embodiment, memory operation unit 130 generates a pipeline ~~stage~~ cycle corresponding to selection of a memory bank in low power instruction memory 103 and a pipeline ~~stage~~ cycle corresponding to instruction readout, only the selected memory bank can be precharged to allow reduction of power consumption. Since pipeline ~~stages~~ cycles IF0-IF2 are effected in parallel, the throughput of low power instruction memory 103 can be improved.

Please amend the paragraph beginning at page 21, line 29 as follows:

Since memory operation unit 130 generates a pipeline ~~stage~~ cycle corresponding to selection of a memory bank of low power data memory 104 and a pipeline ~~stage~~ cycle corresponding to data access, only the selected memory bank is precharged to allow reduction of power consumption. Since pipeline ~~stages~~ cycles M0-M2 are effected in parallel, the throughput of low power data memory 104 can be improved.